IN THE SPECIFICATION

Please modify the paragraph at page 26, lines 7-13, as follows:

When the PRBS signal ~~is sent trough~~ is sent through a band limited transmission line, such as a trace formed on the PCB 100, the PRBS spectrum is altered resulting into ISI. As will be described further with reference to FIGs. 10-22, the high-speed bit stream interface module 102A, 102B, or 102C of the present invention operates in an attempt to fully restore the power spectrum of the PRBS signal therefore eliminating most, if not all of the ISI. The equalized PRBS signal may then be recovered so that even a large ISI residual will be removed and a maximum jitter tolerance may be met.

Please modify the paragraph at page 29, lines 21-23 through page 30, lines 1-5, as follows:

The advantages of such approach are that (1) it allows longer traces on the PCB 100 between C and D and/or cheaper dielectric material for the board construction; (2) it reduces the amount of unfiltered DJ transferred from point C to the transmit point Y; (3) integration of the ~~equalizer 10002~~equalizer 1002, in the same device with the limiting amplifier 1004 and CDR 1006 allows a considerable area saving which is critical in small form factor modules; and (4) the possibility of disabling the operation of the equalizer 1002 and limiting amplifier 1004 independently from the CDR 1006 allows power saving in case they are not needed.

Please modify the paragraph at page 39, lines 17-22, as follows:

The equalizer 1002 of FIG. 14 operates according to the following principles: (1) The input signal is amplified and its amplitude is held constant by the AGC loop 1402; (2) The output of the AGC loop 1402 is fed to two amplifying paths. A first amplifying path includes ~~a low pass filter 1404~~ a low pass filter 1410 that has a flat band response with a -3dB BW > Nyquist and a second amplifying path that includes either band pass or high pass characteristics.